IN THE SPECIFICATION:

Please rewrite the paragraph bridging pages 6 and 7 so that it reads as follows:

Under positive polarity ESD event, as shown in Fig. 4, the P-type substrate or well 28, N-type well 30 and P-type well 32 form an SCR structure with the P+ region 40 embedded in the P-type substrate or well 28 as the anode of the SCR and the N+ region 36 embedded in the P-type substrate or well 28 as the cathode of the SCR. Moreover, the bridge region 42 across the N-type well 30 will lower the breakdown voltage and thus lower the triggering voltage of the induced SCR. When a positive polarity ESD pulse applied on the input pad 44, the junction between the P-type well 32 and N-type well 30 is forward-biased at first. A parasitic PNP transistor 54 appears with the P-type well 32 as its emitter, the N-type well 30 as its base, and the P-type substrate or well 28 as its collector. Due to the P-type substrate or well 28 grounded through the P+ region 34, the vertical PNP transistor 54 is turned on, for the emitter-base is forward-biased and the collector-base is reverse-biased. When the voltage drop across the bridge region 42 and P-type substrate or well 28 reaches the breakdown voltage of the PN junction 52, a plurality of carriers are produced and the produced holes will flow toward the cathode, i.e., P+ region 34. Further, due to the substrate resistance 58, the hole current component will pull high the voltage of the P-type substrate or well 28 to the cathode 34, resulting in the PN junction between the P-type substrate or well 28 and N+ region 36 connected to the cathode forward-biased. This ~~maker~~ makes a parasitic NPN transistor 56 formed with the N+ region 36, P-type substrate or well 28, and N-type well 30, which is turned on with the N+ region 36 as the emitter, the P-type substrate or well 28 as the base, and the N-type well 30 as the collector. Once the parasitic PNP and

NPN transistors 54 and 56 are turned on, the SCR structure will be triggered due to positive feedback procedure, and in Fig. 5 is shown the equivalent circuit 60 of the SCR structure under positive polarity ESD pulse.